Claims

SUB B1

1. A method for forming a semiconductor device comprising first, second and third layers, with a component being formed in the second layer, and first and second etch stop layers being located between the first and second layers, and the second and third layers, respectively, and at least the second etch stop layer being bonded to one of the second and third layers, the method comprising the steps of:

prior to bonding the one of the second and third layers to the second etch stop layer, patterning the second etch stop layer to define the component in the second layer for facilitating etching of the second layer through the third layer,

bonding the one of the second and third layers to the second etch stop layer, and

etching the second layer through the third layer and the second etch stop layer for forming the component in the second layer.

2. A method as claimed in Claim 1 in which a portion of the third layer adjacent the component is etched for exposing the component.

3. A method as claimed in Claim 2 in which the second layer is etched sequentially after the portion of the third layer adjacent the component has been etched in the same etching process.

4. A method as claimed in Claim 2 in which the portion of the third layer adjacent the component which is etched for exposing the component is etched to the second etch stop layer.

5. A method as claimed in Claim 1 in which the second layer is etched to the first etch stop layer for forming the component.

6. A method as claimed in Claim 2 in which a portion of the second etch stop layer adjacent the component and which is exposed by the etched portion of the third layer is etched through the etched portion of the third layer for exposing the component.

7. A method as claimed in Claim 1 in which a portion of the first etch stop layer adjacent the component is etched for forming a void between the component and the first layer after the component has been formed.

8. A method as claimed in Claim 7 in which a communicating bore is formed through the first layer communicating with the first etch stop layer for facilitating etching of the portion of the first etch stop layer adjacent the component for forming the void between the component and the first layer.

SUB B2

9. A method as claimed in Claim 8 in which prior to etching the second layer for forming the component initially only a part of the portion of the first etch stop layer is etched through the communicating bore in the first layer for thinning the first etch stop layer for minimising stresses induced in the portion of the second layer from which the component is to be formed.

10. A method as claimed in Claim 1 in which the first etch stop layer is bonded to one of the first and second layers, and is bonded to the one of the first and second layers prior to the second etch stop layer being bonded to the one of the second and third layers.

11. A method as claimed in Claim 10 in which the second etch stop layer is formed on the second layer after bonding of the first etch stop layer to the respective one of the first and second layers.

12. A method as claimed in Claim 1 in which the first and second etch stop layers are grown layers.

13. A method as claimed in Claim 12 in which the second etch stop layer is grown on the second layer, and the second etch stop layer is bonded to the third layer.

14. A method as claimed in Claim 12 in which the first etch stop layer is grown on the first layer, and the first etch stop layer is bonded to the second layer.

15. A method as claimed in Claim 1 in which each of the first and second etch stop layers which are bonded to an adjacent one of first, second and third layers are bonded to the adjacent layer by annealing.

16. A method as claimed in Claim 15 in which the annealing bonding step is carried out at a temperature in the range of 900°C to 1,200°C.

17. A method as claimed in Claim 16 in which the annealing bonding step is carried out at a temperature in the order of 1,000°C.

18. A method as claimed in Claim 1 in which the first and second etch stop layers are oxide layers.

19. A method as claimed in Claim 1 in which the second etch stop layer is patterned by depositing a photoresist layer on the second etch stop layer and exposing and developing a pattern which defines the component on the photoresist layer, and subsequently etching the second etch stop layer to define the component.

20. A method as claimed in Claim 1 in which the first, second and third layers are of semiconductor material.

21. A method as claimed in Claim 1 in which the first, second and third layers are of silicon material.

22. A method as claimed in Claim 1 in which the first, second and third layers are of single crystal silicon.

23. A method as claimed in Claim 1 in which the component is a micro-mechanical component.

24. A method as claimed in Claim 1 in which the component is a micro-electro-mechanical component.

25. A method as claimed in Claim 1 in which the component is a micro-optical component.

26. A method as claimed in Claim 1 in which the component is a micro-opto-electro-mechanical component.

27. A method as claimed in Claim 1 in which the depth of the first etch stop layer is at least twice the depth of the second etch stop layer.

SUB A2

28. A method for forming a semiconductor device comprising at least a first layer and a second layer with a component formed in the second layer, a first etch stop layer being located between the first and second layers, and a second etch stop layer on the second layer such that the second layer is located between the first and second etch stop layers, the first etch stop layer being of depth greater than the second etch stop layer, the method comprising the steps of:

prior to forming the component in the second layer forming a communicating bore through the first layer communicating with the first etch stop layer adjacent a portion of the second layer where the component is to be formed, and

etching a part of a portion of the first etch stop layer adjacent the portion of the second layer where the component is to be formed for thinning the first etch stop layer adjacent the portion of the second layer where the component is to be formed to an effective stress relieving depth for relieving stress in the portion of the second layer where the component is to be formed.

SUB B4

29. A method as claimed in Claim 28 in which the portion of the first etch stop layer adjacent the component is thinned to a depth relative to the depth of the second etch stop layer for relieving stress in the portion of the second layer where the component is to be formed.

30. A method as claimed in Claim 28 in which the portion of the first etch stop layer adjacent the component is thinned to a depth so that the difference in thicknesses of the respective first and second etch stop layers does not exceed 2

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microns.

31. A method as claimed in Claim 28 in which the portion of the first etch stop layer adjacent the component is thinned to a depth so that the difference in thicknesses of the respective first and second etch stop layers does not exceed 1 micron.

32. A method as claimed in Claim 28 in which the depth of the first etch stop layer is at least twice the depth of the second etch stop layer.

33. A method as claimed in Claim 28 in which the first etch stop layer is bonded to one of the first and second layers.

34. A method as claimed in Claim 28 in which the first etch stop layer is a grown layer.

SUB B5

35. A method as claimed in Claim 28 in which the area in plan view of the portion of the first etch stop layer which is thinned is less than the area in plan view of the component.

36. A method as claimed in Claim 28 in which the area in plan view of the portion of the first etch stop layer which is thinned is at least half the area in plan view of the component.

37. A method as claimed in Claim 28 in which the area in plan view of the portion of the first etch stop layer which is thinned is at least three-quarters the area in plan view of the component.

38. A method as claimed in Claim 28 in which the cross-sectional area of the communicating bore through the first layer is at least half the area of the component in plan view.

39. A method as claimed in Claim 28 in which the component is a micro-

mechanical component.

40. A semiconductor device comprising:

first, second and third layers,

a component formed in the second layer, and

first and second etch stop layers located between the first and second layers, and the second and third layers, respectively, at least the second etch stop layer being bonded to one of the second and third layers, wherein

prior to bonding the second etch stop layer to the one of the second and third layers, the second etch stop layer is patterned to define the component in the second layer for facilitating etching of the second layer through the third layer and the second etch stop layer, and the second layer is etched subsequent to the second etch stop layer having been bonded to the one of the first and second layers.

41. A semiconductor device as claimed in Claim 40 in which a portion of the third layer adjacent the component is etched for forming an opening through the third layer exposing the component.

42. A semiconductor device as claimed in Claim 40 in which a portion of the second etch stop layer adjacent the component is etched for removing the second etch stop layer from the component.

43. A semiconductor device as claimed in Claim 40 in which a portion of the first etch stop layer adjacent the component is etched for removing the first etch stop layer from the component and for forming a void between the component and the first layer.

44. A semiconductor device as claimed in Claim 43 in which the first etch stop layer is etched through a communicating bore formed through the first layer communicating with the first etch stop layer.

45. A semiconductor device as claimed in Claim 40 in which the first and second etch stop layers are oxide layers.

46. A semiconductor device as claimed in Claim 40 in which the first, second and third layers are layers of semiconductor material.

47. A semiconductor device as claimed in Claim 40 in which the first, second and third layers are of silicon material.

48. A semiconductor device as claimed in Claim 40 in which the component is a micro-mechanical component.

49. A semiconductor device as claimed in Claim 40 in which the component is a micro-optical component.